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ISSUING DATE:

2003.01.17

Application NO.: 00804489.9	Applicant: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
Application Date: 2000.12.13	Agent: Ying MU
Title: RADIO BASE STATION DEVICE AND RADIO ...	

THE FIRST OFFICE ACTION
(PCT application for entry into the national phase)

1. ☒ The applicant filed a request for substantive examination on Year ___Month___Day___. According to Article 35 paragraph 1 of the Patent Law, the examiner has conducted a substantive examination to the above-mentioned patent application.

☐ According to Article 35 paragraph 2 of the Patent Law, Chinese Patent Office decided, on its own initiative, to conduct a substantive examination to the above-mentioned patent application.

2. ☒ The applicant requested to take
Year 00 Month 01 Day 14, on which an application is filed with the JP patent office, as the priority date,
Year ___Month___Day___, on which an application is filed with the_____patent office, as the priority date,
Year ___Month___Day___, on which an application is filed with the_____patent office, as the priority date.

3. ☐ The amended document(s) submitted by the applicant is/are not accepted because the said amendment(s) is/are not in conformity with the provision of Article 33 of the Chinese Patent Law.

☐ The Chinese translation of the annexes of the International Preliminary Examination Report.
☐ The Chinese translation of the amendments submitted under Article 19 of PCT .
☐ The amendment(s) submitted under Article 28 or Article 41 of PCT.
☐ The amendment(s) submitted under Rule 51 of The Implementing Regulations of the Patent Law

The concrete reason(s) for not accepting the amendment(S) is/are presented on the text of this Office Action.

4. ☒ The examination has been conducted on the initially filed Chinese translation of the text of the application.

☐ The examination has been conducted on the following text(s) :

☐Specification , page(s)_____ , as originally filed
page(s)_____ , as the annexes of the International Preliminary Examination Report
page(s)_____ , as the amendment(s) submitted under Article 28 or 41 of PCT
page(s)_____ , as the amendment(s) submitted under Rule 51 of The Implementing Regulations of the Patent Law

☐Claim, _____, as originally filed
_____,as the Chinese translation of the amendment(s) submitted under Article 19 of PCT
_____, as the annexes of the International Preliminary Examination Report
_____, as the amendment(s) under Article 28 or 41 of PCT
_____, as the amendment(s) under Rule 51 of The Implementing Regulations of the Patent Law

☐Figure, _____, as originally filed
_____, as the annexes of the International Preliminary Examination Report

_____, as the amendment(s) under Article 28 or 41 of PCT

_____, as the amendments under Rule 51 of The Implementing Regulations of the Patent Law

5. ☒ The following reference document(s) is/are cited by this notification: (the reference numeral(s) thereof will be used in the examination procedure hereafter)

NO.	Reference No. and Title	Publishing Date (or the filing date of rivals)
1	GB 2295 547A	Year 96 month 05
2		Year month
3		Year month
4		Year month

6. Concluding comments

☐ on the specification:

☐ The specification is not in conformity with the provision of Rule 18 of the Implementing Regulations of the Patent Law.

☐ The figures is not in conformity with the provision of Rule 19 paragraph 3 of the Implementing Regulations of the Patent Law.

☐ The specification is not in conformity with the provision of Article 26 paragraph 3 of the Patent Law.

☐ The contents of the application are in contrary to Article 5 of the Patent Law and therefore are not patentable

☒ on the claims:

☐ Claim(s)_____belong(s) to non-patentable subject matter as prescribed in Article 25 of the Patent Law

☐ Claim(s)_____do(es) not possess novelty as requested by Article 22 paragraph 2 of the Patent Law.

☒ Claim(s)_____7_____do(es) not possess inventiveness as requested by Article 22 paragraph 3 of the Patent Law.

☐ Claim(s)_____do(es) not possess the practical applicability as requested by Article 22 paragraph 4 of the Patent Law.

☒ Claim(s)_____1_____do(es) not comply with the provision of Article 26 paragraph 4 of the Patent Law.

☐ Claim(s)_____do(es) not comply with the provision of Article 31 paragraph 1 of the Patent Law.

☒ Claim(s)_____1, 6, 8_____do(es) not comply with the provision of Rule 20 to 23 of the Implementing Regulations of the Patent Law.

☐ Claim(s)_____do(es) not comply with the provision of Article 9 of the Patent Law.

☐ Claim(s)_____do(es) not comply with the provision of Rule 12 paragraph 1 of the Implementing Regulations of the Patent Law.

The detailed analysis for the above concluding comments is/are presented on the text of this Office Action.

7. Based on the above concluding comments, the examiner is of the opinions that:

☒ The applicant should amend the application document(s) in accordance with the requirement as specified in the Office Action.

☐ The applicant should, in his observation, expound the patentability of the application , amend the defects pointed out in the Office Action ; or the application can hardly be approved.

☐ The examiner deems that the application lacks substantive features to make it patentable. Therefore, the application will be rejected if no convincing reasons are provided to prove its patentability.

8.The applicant should pay attention to the following matters:

(1) According to Article 37 of the Patent Law, the applicant is required to submit his observations within four months upon receipt of this Office Action. If the time limit for making response is not met without any justified reason, the application shall be deemed to have been withdrawn.

(2) The amendment(s) made by the applicant must meet the provision of Article 33 of the Patent Law. The amended text should be in duplicate, its format should conform to the related confinement in the Guidance for Examination .

(3). **The observation and the amended document(s) must be mailed or delivered to the Receiving Section of the Chinese Patent Office. No legal effect shall apply for any document(s) that not mailed to or reached the Receiving Section.**

(4) Without being invited, the applicant and/or the agent should not go to the Chinese Patent Office to interview an examiner.

9. The text of this Office Action contains_1_ page(s), and has the following attachment(s):

☐ _____copies of the cited references, total_____pages.

Examination Section No. _____ Examiner _____ Seal of Examination Dept. .For business only (if the Office Action wasn' t stamped by the specified seal, it has no legal effect)

00804489.9

Text of the First Office Action

The present application for a patent for invention provides an apparatus and a method that are capable of achieving AAA receiving by a RACH and AAA transmission by an AICH. The examiner provides the following examination opinions according to the original filed Chinese version of the international application.

Claim 1 is for a wireless base station apparatus. However, the specification text and figures do not disclose its technical features of "a correlation level detecting means" and "detecting means", but only discloses a level detection circuit and a RACH preamble detection circuit. Thus, the technical solution sought for protection in claim 1 is not supported by the specification in essence, which does not comply with the provision that the claims shall be supported by the specification as prescribed in Article 26, paragraph 4 of the Chinese Patent Law. Furthermore, since the object of the present invention is to achieve AAA receiving by a RACH and AAA transmission by an AICH, "a plurality of directivity patterns that have been set in advance" disclosed in the technical solution of the specification should be the indispensable technical feature. Accordingly, the direction of arrival estimation circuit, the receiving weight calculation circuit, the delay profile circuit and the like disclosed in the specification should be added into claim 1, so as to make the technical solution sought for protection in claim 1 comply with the provision that the independent claim shall outline the technical solution of an invention and state the essential technical features necessary for the solution of its technical problem as prescribed in Rule 21, paragraph 2 of the Implementing Regulations of the Chinese Patent Law.

Claim 6 is for a communication terminal apparatus for carrying out wireless communication with a wireless base station apparatus. However, the characterizing portion of said claim makes definition to the base station, but fails to define the subject matter of "communication terminal apparatus" that it claims to protect, which renders the technical solution sought for protection in claim 6 unclear. Thus, it does not comply with the provision that the claims shall define clearly the scope sought for protection as prescribed in Rule 20, paragraph 1 of the Implementing Regulations of the Chinese Patent Law.

Claim 7 is for a communication terminal apparatus. However, Reference 1 has disclosed a RAKE combiner/despreader apparatus for use in a direct sequence spread spectrum communication system, wherein disclosing (refer to page 3, line 12 to page 4, line 21 of the specification and Fig. 1) a RAKE combiner/despreader apparatus having channel estimators. Since it is obvious for those skilled in the art that the communication terminal of the CDMA system comprises the despreading means, channel estimating means and demodulating means, the technical solution sought for protection in claim 7 does not possess inventiveness as prescribed in Article 22, paragraph 3 of the Chinese Patent Law. Accordingly, the applicant should define concretely the improvement for the structure of the communication terminal apparatus, and describe said communication terminal apparatus with the structure technical features or the structure & functional technical features.

Claim 8 refers to claim 7. However, its characterizing portion is not added with new technical feature, but only defines the signal used in the channel estimation. Thus, since the claim to which it refers does not possess inventiveness, the technical solution sought for protection in claim 8 does not comply with the provision that the dependent claim shall further define the claim to which it refers by additional technical features

as prescribed in Rule 21, paragraph 3 of the Implementing Regulations of the Chinese Patent Law.

Based on the above reasons, the application can not be granted a patent right under the present text. If the applicant makes amendments to the application and submits the new claims and specification in accordance with above examination opinions within the specified time limit, the present application will have a prospect of being granted a patent right. And any amendment should not go beyond the scope of the original specification and claims so as to comply with the provision of Article 33 of the Chinese Patent Law.

PIMY 0998A

中华人民共和国国家知识产权局

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张慧 印 审查员

（无审查业务专用章，不具备法律效力）

专利局 2003.1.17 发文

申请号：00804489.9	部门及通知书类型：3--D	发文日期：
申请人：	松下电器产业株式会社	
发明名称：	无线基站装置和无线通信方法	

第一次审查意见通知书

（进入国家阶段的 PCT 申请）

1. ☒ 依申请人提出的实审请求，根据专利法第 35 条第 1 款的规定，审查员对上述发明专利申请进行实质审查。
   ☐ 根据专利法第 35 条第 2 款的规定，国家知识产权局决定自行对上述发明专利申请进行审查。
2. ☒ 申请人要求以其在：
   JP 专利局的申请日 2000 年 1 月 14 日 为优先权日，
   _____ 专利局的申请日 _____ 为优先权日，
   _____ 专利局的申请日 _____ 为优先权日，
3. ☐ 申请人提交的下列修改文件不符合专利法第 33 条的规定，因而不能接受：
   ☐ 国际初步审查报告附件的中文译文。
   ☐ 依据专利合作条约第 19 条规定所提交的修改文件的中文译文。
   ☐ 依据专利合作条约第 28 条或 41 条规定所提交的修改文件。
   ☐ 依据专利法实施细则第 51 条规定所提交的修改文件。
   修改不能被接受的具体理由见通知书正文部分。
4. ☒ 审查是针对原始提交的国际申请的中文译文进行的。
   ☐ 审查是针对下述申请文件进行的：
   说明书 第_____页，按照原始提交的国际申请文件的中文译文；
   第_____页，按照国际初步审查报告附件的中文译文；
   第_____页，按照依据专利合作条约第 28 条或 41 条规定所提交的修改文件；
   第_____页，按照依据专利法实施细则第 51 规定所提交的修改文件。
   权利要求 第_____项，按照原始提交的国际申请文件的中文译文；
   第_____项，按照依据专利合作条约第 19 条规定所提交的修改文件的中文译文。
   第_____项，按照国际初步审查报告附件的中文译文；
   第_____项，按照依据专利合作条约第 28 条或 41 条所提交的修改文件；
   第_____项，按照依据专利法实施细则第 51 条规定所提交的修改文件。
   附图 第_____页，按照原始提出的国际申请文件的中文译文；
   第_____页，按照国际初步审查报告附件的中文译文；
   第_____页，按照依据专利合作条约第 28 条或 41 条所提交的修改文件；
   第_____页，按照依据专利法实施细则第 51 条规定所提交的修改文件。

第一次审查意见通知书正文

本发明专利申请提供一种可以实现 RACH、AICH 的 AAA 接收和发送的装置和方法，审查员根据原始提交的国际申请中文译本作出如下审查意见：

权利要求 1 请求保护一种无线基站装置，其中的技术特征“相关电平检测部件”以及“检测部件”在说明书文字及附图部分均未出现，仅仅存在电平检测电路以及 RACH 前置码检测电路，因此，权利要求 1 所请求保护的技术方案实质上得不到说明书的支持，不符合专利法第 26 条第 4 款有关权利要求书应当以说明书为依据的规定。此外，由于本发明目的是实现 RACH、AICH 的 AAA 接收和发送，因此，说明书公开的技术方案中的“预先设定的多个方向性图案”应当是必要技术特征，因此，应当将说明书中的到来方向估计电路、接收加权运算电路、延迟分布形成电路等加入到权利要求 1 中，使权利要求 1 所请求保护的技术方案符合专利法实施细则第 21 条第 2 款有关独立权利要求应当从整体上反映发明的技术方案，记载解决技术问题的必要技术特征的规定。

权利要求 6 请求保护一种与无线基站装置进行无线通信的通信终端装置，该项权利要求的特征部分是对基站进行了描述，对于其所请求保护的主题“通信终端装置”并没有进行限定，因此导致权利要求 6 所请求保护的技术方案不清楚，不符合专利法实施细则第 20 条第 1 款有关权利要求书应当清楚的表述请求保护的范围的规定。

权利要求 7 请求保护一种通信终端装置，对比文件 1 中公开了一种用于直接序列频谱扩展通信系统的 RAKE 合成/解扩装置，其中公开了（见说明书第 3 页第 12 行至第 4 页第 21 行，附图 1）具有信道估计器的 RAKE 合成/解扩装置，由于在 CDMA 系统的通信终端中存在解扩部件、信道估计部件以及解调部件对于本领域普通技术人员来说是显而易见的，因此权利要求 7 所请求保护的技术方案不具备专利法第 22 条第 3 款有关创造性的规定。申请人应当具体写明其对于通信终端装置的结构上的改进，采用结构技术特征或结构和功能相结合的技术特征对该通信终端装置进行描述。

权利要求 8 引用权利要求 7，但其限定部分并没有增加新的技术特征，仅仅规定了信道估计中所用的信号，因此，在其引用的权利要求不具备创造性时，权利要求 8 所请求保护的技术方案不符合专利法实施细则第 21 条第 3 款有关从书权利要求应当用附加的技术特征对引用的权利要求做进一步限定的规定。

基于上述理由，本申请按照目前的文本还不能被授权，若申请人根据上述审查意见在规定期限内对本申请进行修改，提交新的权利要求书和说明书，则本申请可望被授予专利权，且修改时应满足专利法第 33 条的规定，不得超出原说明书和权利要求书的记载范围。

审查员：张慧　　电话：62093785

Rake combiner/despreader apparatus

Patent Number: GB2295527
Publication date: 1996-05-29
Inventor(s): HULBERT ANTHONY PETER
Applicant(s): ROKE MANOR RESEARCH (GB)
Requested Patent: ☐ GB2295527
Application Number: GB19940023935 19941126
Priority Number(s): GB19940023935 19941126
IPC Classification: H04L27/22; H04B1/69
EC Classification: H04B1/707F3
Equivalents:

Abstract

The Rake combiner/despreader apparatus comprises a shift register 2 for receiving channel estimates. The channel estimates are stored temporarily in two register banks 24, 22 which respectively store the real channel estimates and the imaginary channel estimates. The output of the register banks are applied to a respective adder/subtractor circuit 18, 26 and the respective channel estimates are included in the addition/subtraction under the control of control circuits 16 which compare the bit reference from the shift register to the output of a modulo N counter 4. The output of the counter 4 represents an index for the received bit corresponding to the position of the chip specified in a real or imaginary chip sequence which is applied to the shift register 2. The outputs from the respective adder/subtractor circuits 18, 26 are passed through a respective combiner circuit 28, 30 which combines the output with the real or imaginary channel samples respectively. The output of the combiner circuits 28, 30 are added together in an adder 32. An accumulator is provided for each bit position, and the output from the adder 32 is applied to an input of the particular accumulator 14, by a switch 38. The inputs to the accumulator 14 is formed by the output of the adder circuit 32 in combination with the selected output from the accumulator 14. The output of the accumulator 14 is selected by switch 36. When the last sample which can influence a particular bit has been processed, the contents of the accumulator 14 are read out and fed to subsequent circuitry for appropriate processing.

Claims

CLAIMS

1. A Rake combiner/despreader apparatus, for use in a spread spectrum system, the apparatus comprising means for obtaining channel estimates, storage means for holding said channel estimates, controlling means for controlling the passage of data from the storage means to calculation means arranged to add or subtract said channel estimates and generate an output signal which is applied to combining means arranged to combine said output signal with a channel sample.

2. Apparatus as claimed in Claim 1, wherein the storage means comprises a first register bank for receiving real channel estimates and a second register bank for receiving imaginary channel estimates.

3. Apparatus as claimed in Claim 1 or Claim 2, wherein said controlling means comprises a store holding a current part of a spread spectrum chip sequence derived from a local generator and references to bits which are currently being despread, and a plurality of control circuits each connected to a respective chip position of said store, so that, for each chip position the control circuit connected thereto performs a comparison between the bit reference and all current bit references, and if equality is found the corresponding stored channel estimate is passed to said calculation means.

4. Apparatus as claimed in Claim 3, wherein the value of the corresponding stored chip determines whether the relevant channel estimate is added or subtracted in the calculation means.

5. Apparatus as claimed in Claim 3 or Claim 4 wherein said store is a shift register.

6. Apparatus as claimed in any of the preceding Claims 3,4 or
S wherein said store is connected to a first modulo counting means driven by a clock generator via a divider circuit representing a spreading factor, said modulo counting means providing an index for each received bit corresponding to the position of an appropriate real chip.

7. Apparatus as claimed in any preceding Claim, wherein the calculation means comprises first and second add/subtract tree circuits, an output of each being respectively connected to a combiner means arranged to combine the output of the calculation means with the channel sample.

8. Apparatus is claimed in Claim 7, wherein an output of each combiner means is applied to a first adder and accumulated on a bit by bit basis in an accumulator.

9. Apparatus as claimed in Claim 8, wherein the input to the accumulator comprises a combined signal generated from a second adder which receives at a first input, an output from said first adder, and at a second input, a selected output from said accumulator.

10. Apparatus as claimed in Claim 9 wherein the input to the accumulator is to a selected bit position.

11. Apparatus as claimed in Claim 10, wherein the input and output selection to/from the accumulator is controlled by switching means controlled by an output of a second modulo counting means driven via a master clock.

12. Apparatus as claimed in any preceding claim which utilises binary phase shift keying modulation.

13. Apparatus as claimed in any of the preceding Claims 1 to 11 which utilises quaternary phase shift keying modulation.

14. Apparatus substantially as herein before described with reference to the accompanying drawings.

Description

RAKE COMBINER/DESPREADER APPARATUS

The present invention is concerned with a Rake combiner/despreader apparatus for the demodulation of direct sequence spread spectrum (DSSS) signals in a multipath environment using so called Rake technology.

The Comprehensive Rake Receiver as described in pending patent application number 9316489.5 involves sampling the filtered complex baseband signal at one chip intervals and creating a digital matched filter to the channel (Rake filter) in which all of the multipath components are combined in a maximal ratio sense. The signal is also despread. In the prior art there are two approaches to this problem. The traditional approach despreads the individual multipath components, then scales them according to the path levels and then adds them together. The pre-combining approach as described in co-pending patent application number 9213535.9 weights and combines the multipath components at the chip level prior to despreading them.

The traditional approach is useful where there is only a small number of Rake fingers and where only one spread spectrum code, transmitted over the common path, needs to be demodulated.

The pre-combining approach is useful where many signals need to be demodulated. It is, however, rather complicated.

An aim of the present invention is to provide a combiner/despreading apparatus which allows many Rake fingers to be combined but has modest complexity. Typically the multiplication rate is the same as for the traditional approach but the multiplication is by the samples on one port (which are typically only four bits precision), leading to a lower complexity multiplier.

According to the present invention there is provided a Rake combiner/despreader apparatus, for use in a spread spectrum system, the apparatus comprising means for obtaining channel estimates, storage means for holding said channel estimates, controlling means for controlling the passage of data from the storage means to calculation means arranged to add or subtract said channel estimates and generate an output signal which is applied to combining means arranged to combine said output signal with a channel sample.

According to an aspect of the invention the storage means comprises a first register bank for receiving real channel estimates and a second register bank for receiving imaginary channel estimates.

According to a further aspect of the invention the controlling means comprises a store holding a current part of a spread spectrum chip sequence derived from a local generator and references to bits which are currently being despread, and a plurality of control circuits each connected to a respective chip position of said store, so that, for each chip position the control circuit connected thereto performs a comparison between the bit reference and all current bit references, and if equality is found the corresponding stored channel estimate is passed to said calculation means.

According to yet a further aspect of the invention the value of the corresponding stored chip determines whether the relevant channel estimate is added or subtracted in the calculation means.

An embodiment of the invention will now be described with reference to the accompanying drawings wherein:
Figure 1 shows a block diagram of a combiner/despreader apparatus, and,
Figure 2 shows an example of a control circuit shown in
Figure 1.

The combiner/despreader circuit shown in Figure 1 comprises a shift register 2 connected to receive a reference clock from a modulo N counter 4. A real chip sequence signal is generated by a generator 44 and duplicates the transmitted real chip sequence signal, and is received at a further input 6 of the shift register. A respective bit of the shift register 2 is connected to an input of a control circuit 16 respectively, which receives at a further input thereof, an output signal from a second modulo N counter 12. An output from each of the control circuits 16 is connected to an input of a register bank 22 and an input of a register bank 24. The register bank 22 handles imaginary channel estimates and the register bank 24 handles real channel estimates. The real and imaginary channel estimates are generated from channel estimators 40, 42 respectively.The real channel estimates are applied to an add/subtract tree circuit 18, and the imaginary channel estimates are applied to an add/subtract tree circuit 26. A master clock circuit 8 drives the modulo N counter 12 and the modulo N counter 4. The output of the master clock circuit 8 is passed to a divide by N circuit 10 and is further divided by a divide by H circuit 20 prior to application to the module N counter 4. The divide by H circuit represents the spreading factor. The output from each add/subtract tree circuit 18, 26 is connected to an input of a combiner circuit 28 ,30 respectively. The combiner circuit 28 combines the output of the add/subtract tree circuit 18 with the real channel samples, and the combiner circuit 30 combines the output of the add/subtract tree circuit 26 with the imaginary channel samples.The output generated from each of the combiner circuits 28, 30 is applied to an adder circuit 32, the output of which is applied to an input of a further adder circuit 34. N accumulators, 14 one for each bit currently being processed have a switch 36 connected to the output of each accumulator and a switch 38 connected to the input of each accumulator. The switch 36 selects which bit is to be connected to the adder circuit 34, the output of which is connected back to the switch 38 and is fed back to an input of a particular bit position in the accumulator 14. The switches 36, 38 are

controlled by the output of the modulo N counter 12.

The operation of Figure 1 will now be described in conjunction with Figure 2 which shows an example of one of the control circuits 16.

The fundamental principle is to take the incoming complex baseband samples and determine their contribution (by despreading and by channel matched filtering) to every bit that they may be derived from. Each received sample comprises noise and interference plus components derived from several transmitted chips, each subjected to a path delay. Thus, suppose the sampled response throught the transmitter pulse shaping filter, channel and receiver filter for a radio link can be described as:

and suppose that the chip sequence is:

If the spreading factor is H then the bit sequence can be set as:

Where br is the rth transmitted bit. This is a set H identical impulses, bipolar modulated with data, at the chip rate for every bit.Thus the actual transmitted sequence is then:

Then the received sequence of samples is:

Thus, the signal component in the nth sample can be written as:

where the subscript, v = #n - i#
H
Thus, if the nth received sample is Y(n), a matched filtering operation can be performed for every sample by forming Y(n).S*(n). In fact, because of the modulation, various S(n) must be formed over summation values for which v is constant.

Thus vO = FHI gives the sample's contribution to the matched filter accumulation for the newest bit bvo
This is obtained as

where âi is an estimate of aj.

The contribution to the previous bit bX,I is given by:

And to the bit before, by

and so on....

The last contribution ends when i reaches L-1. Thus the maximum number of bits which can contribute to one sample is N =1+ FHH.

The maximum significant delay span for assumed for the channel,
Lmax chips must be determined. Then for a given spreading factor,
H, the number of bits, N to be handled in parallel can be determined.

The complexity of the receiver will depend upon the form of spreading and on the basic modulation. The simplest form is real-only spreading - ie q;=0 for all k. The simplest form of modulation is BPSK in which only the real part of Y(n) .S*(n) need be calculated.

One implementation for the case of real-only spreading and
BPSK modulation based on these principles is shown in Figure 1.

It is assumed that channel estimates have already been derived over the delay spread of the signal (either using a pilot signal or from the data signal through decision direction).

The process is half complex, therefore much of the hardware is repeated and shown symmetrically. For simplicity, only the left hand side (the real part) will be described. Essentially, the circuit operates for each sample (taken at the chip rate) to accumulate, sequentially, chip contributions for each of the pertinent N transmitted bits. Thus the master clock rate is N/Tc.

The shift register 2 is several bits wide. It will be appreciated that a further shift register would need to be provided for the Q imaginary channel which would receive the imaginary chip sequence in the case of quaternary phase shift keying (QPSK) spreading. These bits are arranged to consist of two components:

One bit corresponding to the appropriate real chip, and Llog7NJ bits, together forming an index for the received bit corresponding to the position of the chip specified in the bit corresponding to the appropriate real chip. These latter bits are provided by the modulo N counter 4 which is driven from a divide by H circuit 20 (the spreading factor) from the chip sample clock, generated from the master clock 8 and divided by N in circuit 10.

The modulo N counter 12 from the master clock 8 and the divide by N circuit 10 cycles through the reference numbers for all output bits (in this case three). Its output, in turn, therefore makes connections to the inputs and outputs of the relevant M bit accumulator circuit 14. Additionally, the output of counter 12 is applied to the control circuits 16, the operation of which is shown in Figure 2.

The control circuit detects when a given chip corresponds to the bit which is currently active by comparing in a comparator 50, the bit reference from the shift register 2 with the output of the modulo N counter 12 and causes the "Include" line to be activated so that corresponding channel estimates will be included in the summation. It also passes the Chip value from the shift register circuit. This will have the effect of either passing the relevant channel estimate to the adder/subtractor tree circuit 18, 20 or of 2's complementing it first (for subtraction).

Thus, the control lines pass into the registers holding the real channel estimates and control their output in to the adder/subtractor tree circuit. This produces, in turn the summations of equations 1, 2, 3 etc. The matched filtering operation is then performed taking the real and imaginary complex samples, and multiplying and adding them. The values are then summed into the appropriate M bit accumulator 14.

When the last sample which can influence a particular bit has been processed, the contents of the bit accumulator are read out and fed to subsequent circuitry for appropriate processing (eg decisions, de-interleaving, soft error correction decoding) according to the original operations applied prior to modulation in the transmitter. After the accumulator output is read out, it is reset to zero and assigned to the next bit in the sequence.

It will be appreciated that if the spreading is complex, most of the hardware will need to be duplicated to recover the bit energy from the Qchannel signal component. Moreover, if the modulation is complex, further duplication will be needed to recover the complex decision variable.
